A 0.4-V, 90 ∼ 350-MHz PLL With an Active Loop-Filter Charge Pump

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***Abstract*—A 0.4-V phase-locked loop (PLL) that has much improved power efficiency is realized in standard 65-nm CMOS. The PLL employs a novel ultralow-voltage charge pump that compensates current mismatch with an active loop filter and produces significantly reduced reference spurs. Its voltage-controlled oscillator (VCO) is designed with the body-bias technique and includes an automatic frequency calibration circuit that provides low VCO gain and wide tuning range. The PLL output frequency can be tuned from 90 to 350 MHz. At 350-MHz output, the PLL consumes 109 μW, which corresponds to the power efficiency of 0.31 mW/GHz.**

***Index Terms*—Active-loop filter (ALF), body-bias technique, charge pump (CP) current matching, phase-locked loop (PLL), power efficiency, reference spur, ultralow voltage (ULV).**

I. Introduction

THERE is an increasing demand for ICs to have reduced power consumption and enhanced power efficiency. The most effective method of reducing power consumption is by lowering supply voltages. International Technology Roadmap for Semiconductors predicts that the operating supply voltage will be reduced to 0.5 V within a decade and further to 0.43 V by 2026 [1]. Consequently, ultralow-voltage (ULV) IC design techniques have been actively investigated [2]–[4]. In addition, ULV realization of the mixed-signal circuits such as phase-locked loops (PLLs), which is an essential block for many system-on-chip applications, is of significant research interest. Several ULV PLLs have been reported [5]–[8] with very small power consumption. However, their power efficiencies, defined as the power consumption divided by the output frequency, are larger than 1 mW/GHz.

In an effort to further improve PLL power efficiency, we investigate a 0.4-V PLL in 65-nm CMOS technology. For this, we optimize each PLL block for ULV operation. In particular, we propose a novel charge pump (CP) structure suitable for ULV operation with good current matching characteristics. The resulting PLL achieves 90- to 350-MHz operation with 0.4-V supply voltage with power efficiency of 0.31 mW/GHz at 350 MHz.

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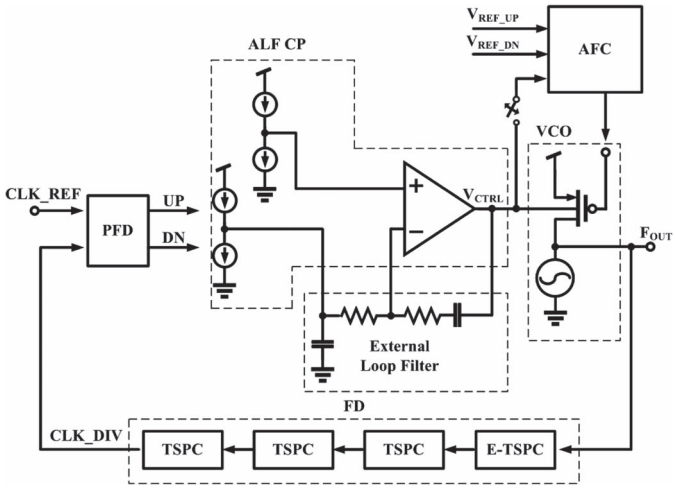

Fig. 1. Proposed PLL architecture.

This brief is organized as follows. In Section II, the overall PLL architecture is described and details of each building block are explained. Section III presents the measurement results and the conclusion is given in Section IV.

II. PLL Architecture

Fig. 1 shows our PLL architecture. It consists of a conventional D-flip flop (DFF)-based phase-frequency detector (PFD), a CP with an active-loop filter (ALF), a pseudodifferential ring-based voltage-controlled oscillator (VCO), and an automatic frequency calibration (AFC) circuit. It also includes a divide-by-16 frequency divider (FD) consisting of an extended true-single-phase-clock DFF [9] for fast operation and three stages of true-single-phase-clock DFFs [10] for low power consumption.

A. CP With an ALF

CP design with a ULV supply is particularly challenging due to its limitation in using multiple-stacked transistors and nonideal CP behaviors such as current and timing mismatch [11]. Mismatch in CP charging and discharging currents generates PLL phase offset and increases reference spurs. Several single-ended mismatch-free CPs have been reported [12]–[15], but they cannot operate with ULV supplies due to the voltage headroom limitation. Differential CPs with ALFs have been reported [16]–[18], which can effectively eliminate mismatches in CP, but they require multiple-stacked transistors with additional compensating circuits for differential operation that consume a large amount of power. In [8], the dynamic-threshold CMOS technique is utilized to overcome the voltage headroom

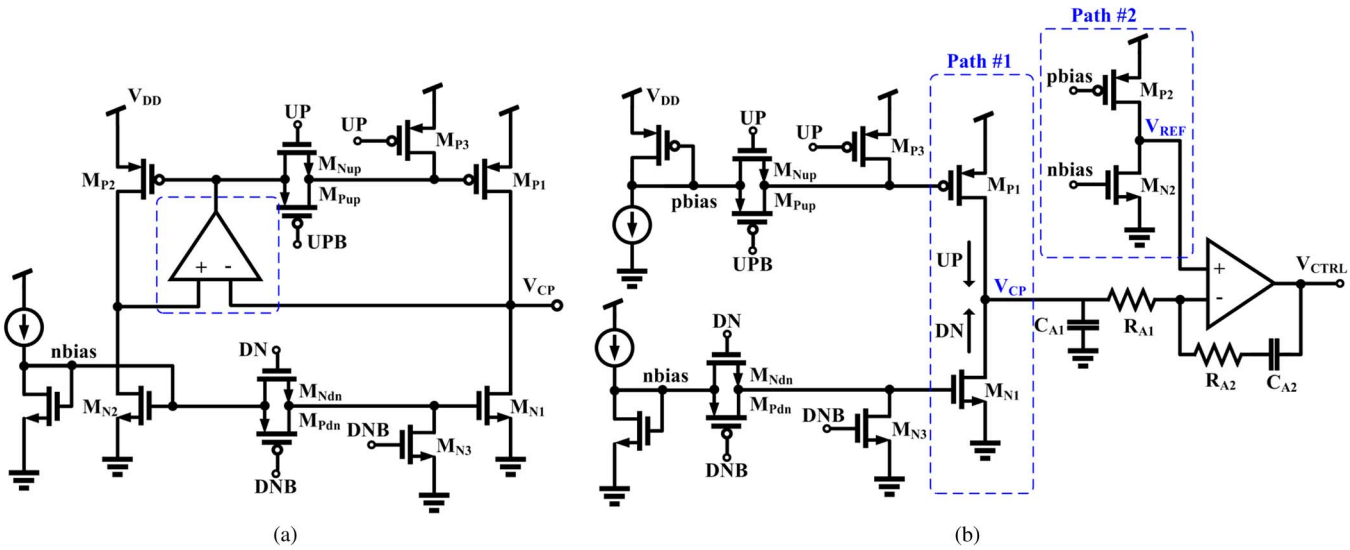

Fig. 2. ULV CP with current matching technique: (a) 2-stacked CP with negative feedback and (b) Proposed CP with ALF.

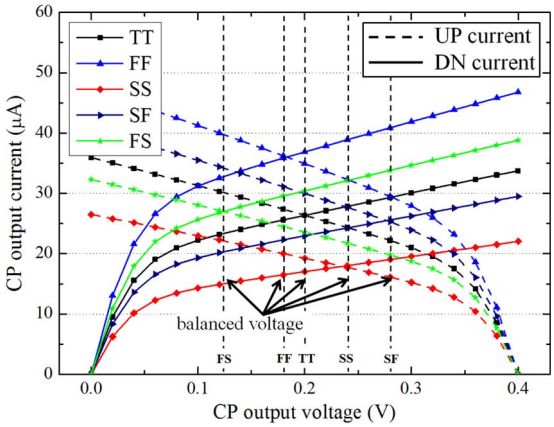

Fig. 3. Simulated CP output current against CP output voltage for different process corners.

problem. However, this requires triple-well CMOS processes, and a further reduction in supply voltage is not easy. In [5] and [7], gate-switching structures with two-stacked transistors are used. Although they work with ULV supplies, they are vulnerable to mismatch in charging and discharging currents.

This problem can be solved with two-stacked CP by applying a negative feedback with an operational amplifier (Op-amp), as shown in Fig. 2(a). However, the structure requires an Op-amp with a very high slew rate for achieving a fast switching operation with large transistors. In order to ease this OP-amp burden, a novel CP structure is proposed, as shown in Fig. 2(b). The fixed bias voltages (pbias, nbias) can cause significant mismatch between UP and DN currents depending on CP output voltage, $\mathrm{V_{CP}}$, as well as process, voltage, and temperature (PVT) variation, as shown in Fig. 3. However, if $\mathrm{V_{CP}}$ is fixed to a specific value that balances UP and DN currents, as marked in Fig. 3, current mismatch can be eliminated, which can be achieved with an ALF.

With the ALF, V_{CP} is isolated from VCO control voltage V_{CTRL} and follows the reference voltage. The CP output current path (Path #1) is duplicated to the replica path (Path #2), and the same nbias and pbias voltages are applied to both paths. Because the switching CMOS in Path #2 (M_{P2}, M_{N2}) are always turned on, V_{REF} is at the value that makes the current through M_{P2} and M_{N2} identical. With the OP-amp, V_{CP} follows V_{REF} and, finally, UP and DN currents in Path #1 are matched regardless of PVT variation. We designed the two paths with transistors having the same sizes and did very careful layout, so that the reference spur due to mismatch between path 1 and path 2 can be minimized.

Fig. 4(a) shows simulation results of CP output currents, and Fig. 4(b) shows the dependence of V_{CP} and V_{REF} on nMOS bias current variation for different process corners. Even if we force extra nMOS bias currents to cause mismatch, UP and DN currents are same and V_{CP} is equal to V_{REF} as long as the OP-amp has enough gain. The OP-amp has a configuration of a two-stage nMOS mirror, so that the rail-to-rail operation can be achieved without any voltage headroom problem.

CP gate switching also affects the reference spur. Due to parasitic capacitance of switches and bias transistors, the clock feedthrough generates peak currents for rising and falling edges during up/down switching activities. We carefully determined CP transistor sizes and the output slope of PDF to minimize unwanted switching feedthrough.

The proposed architecture has several advantages. First, the Op-amp does not need to have as high a slew rate as in Fig. 2(a), resulting in power reduction. Although the CP output pulses can have high-frequency components, they can be filtered by a low-pass filter before the OP-amp and, consequently, the OP-amp can be relieved from the high slew-rate requirement. Second, the VCO control voltage V_{CTRL} can swing the full supply range regardless of CP output voltage V_{CP}. In the case of the PLL based on a passive loop filter, V_{CP} is equal to V_{CTRL}. Thus, if CP provides a narrow voltage range, then the VCO output range is also restricted.

B. VCO With an AFC

The VCO is another important building block for ULV PLL. A ring VCO is used in our PLL since the LC VCO at the

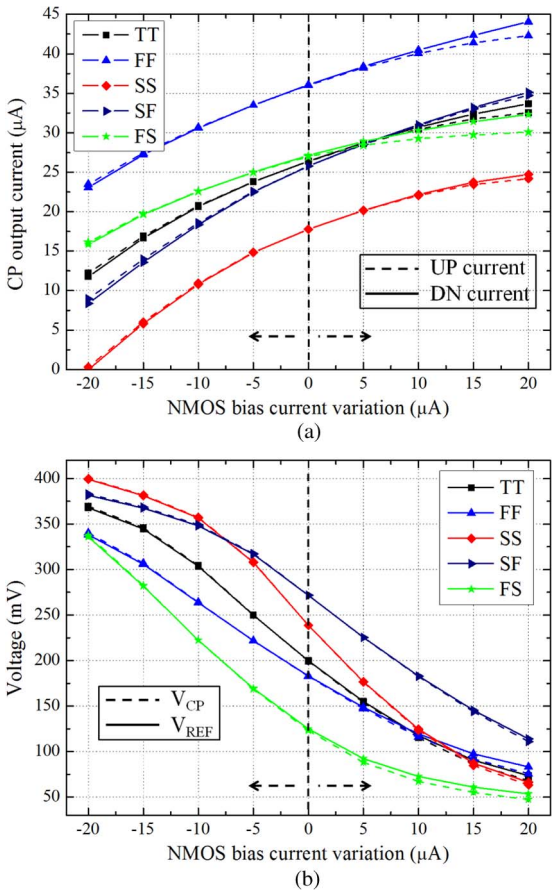

Fig. 4. Simulation of (a) CP output current, and (b) V_{CP} and V_{REF} voltage against NMOS bias current variation for different process corners.

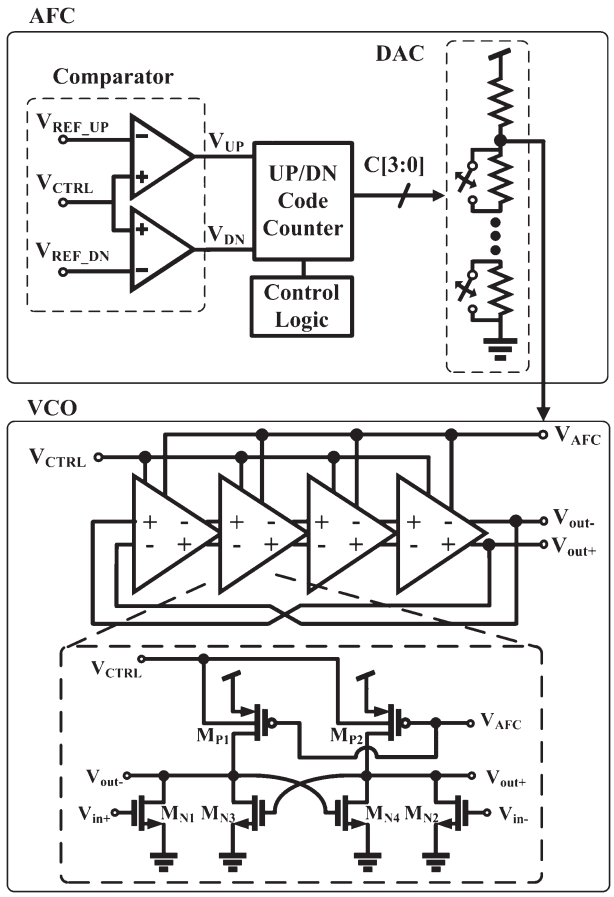

Fig. 5. VCO with AFC circuit.

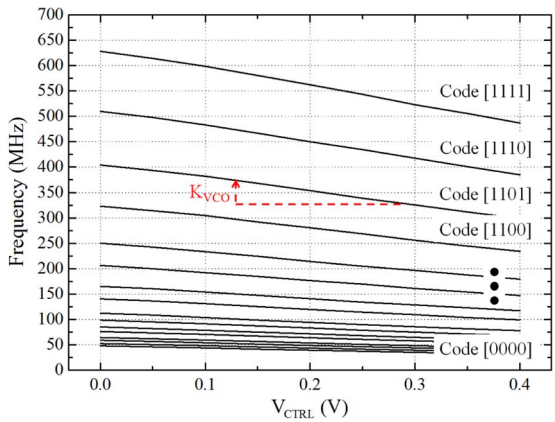

Fig. 6. Simulated VCO tuning range with different AFC codes.

target frequency of hundreds megahertz occupies a very large chip area. There are several challenges for ring ULV VCO implementation. One is limitation in using multiple-stacked transistors, which restricts VCO output frequency. Another is VCO frequency dependence on PVT variation, which becomes very significant with ULV supply [3]. Therefore, the VCO must have a wide enough tuning range to ensure the target frequency operation requiring large VCO gain K_{VCO}. However, this results in degraded PLL phase performance.

For our design, we employ two-stacked nMOS feedback delay cell reported in [7] with the body-bias technique that provides linear and low K_{VCO}. In addition, an AFC circuit is added, which provides a wide tuning range. Fig. 5 shows our VCO with an AFC circuit. The VCO receives two input signals V_{CTRL} and V_{AFC}. V_{CTRL} is the fine-tuning signal from the ALF and V_{AFC} is the digitally controlled coarse-tuning signal from the AFC. In the AFC block, a resistor-ladder network digital-to-analog converter (DAC) is used for low-power dissipation after PLL is locked. The AFC block compares V_{CTRL} with two threshold voltages $V_{\mathrm{REF\_UP}}$ and $V_{\mathrm{REF\_DN}}$ [19]. The result of this comparison changes the built-in 4-bit code counter. Once VCO output reaches the target frequency region, the control circuit stops counting and saves the codes to the latches that control the DAC for the desired V_{AFC}. The simulated VCO tuning range with different AFC codes are shown in Fig. 6. K_{VCO} varies from 60 to 375 MHz/V in simulation when the AFC code changes from 0000 to 1111. The VCO provides linear and low K_{VCO}, and the AFC circuit offers a wide frequency tuning range.

III. Measurement Result

Our PLL is fabricated with standard 65-nm CMOS technology and is mounted on an FR4 board for measurement. The reference frequency is provided by a signal generator, and the PLL output is measured by an oscilloscope and a spectrum analyzer. Fig. 7 shows a die microphotograph and the layout. The total area is about 0.0081 mm^2, excluding the off-chip loop filter.

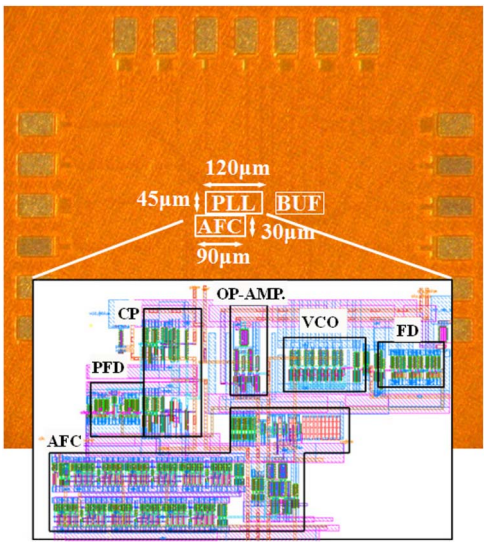

Fig. 7. Microphotograph and layout of the PLL.

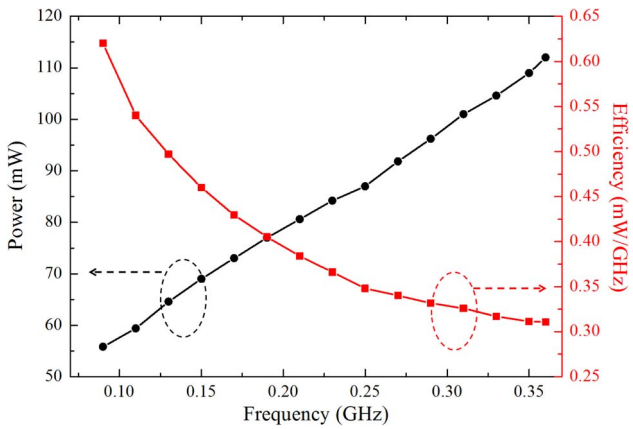

Fig. 8. Measured power consumption and power efficiency with different output frequency.

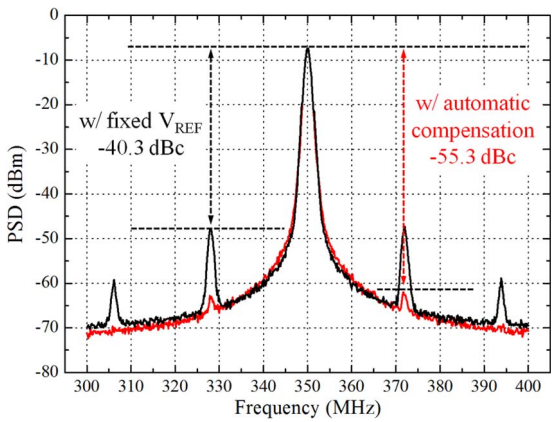

Fig. 9. Measured output spectra at 350 MHz: with the fixed CP reference voltage (0.25 V) and with automatic compensation.

Fig. 8 shows the measured PLL power consumption and power efficiency with varying output frequencies. Since our PLL has the fixed division ratio of 16, the PLL output frequency is controlled by changing the reference frequency. With 5.625- to 21.875-MHz reference input, the PLL generates 90- to 350-MHz output with increasing power efficiency. The low-frequency operation is limited by the loop bandwidth, but the limiting factor for high-frequency operation is not identified.

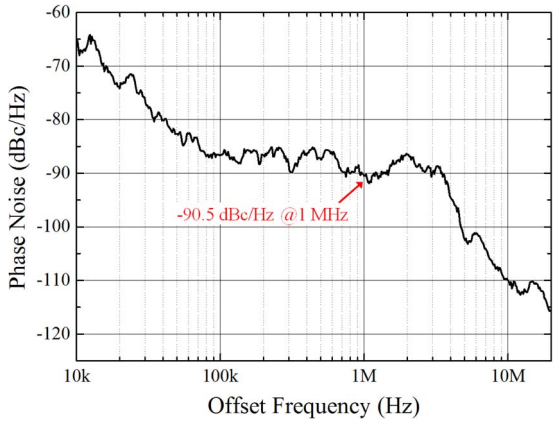

Fig. 10. Phase noise of the PLL at 350 MHz.

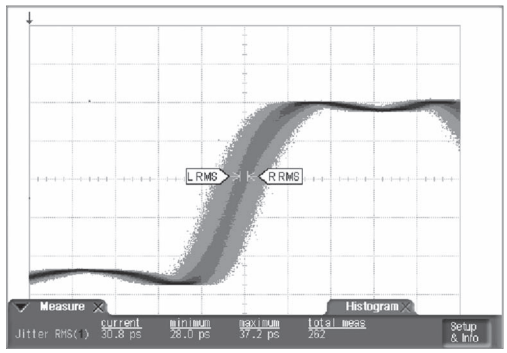

Fig. 11. Measured timing jitter of the PLL at 350 MHz.

TABLE I
POWER BREAKDOWN

Total Power @ 0.4V, 350 MHz	109 uW
PFD	1.04 uW
CP	12.7 uW
VCO	54.4 uW
FD	15.1 uW
ALF	14.0 uW
AFC	8.68 uW
Others	2.8 uW

Fig. 9 shows the measured PLL output spectra at 350 MHz with the fixed CP reference voltage V_{REF} at 0.25 V and with automatic compensation. The reference spur is -40.3 dBc with fixed V_{REF} and -55.3 dBc with automatic compensation. Fig. 10 shows the measured phase noise of our PLL at 350-MHz output frequency. Its phase noise is -90.5 dBc/Hz at 1-MHz offset. Fig. 11 shows the measured jitter characteristics also at 350 MHz. The RMS jitter is 30.8 ps (0.01 UI).

Table I shows the power consumption for each PLL block with 0.4-V supply. The overall power consumption is 109 μW at 350-MHz output frequency, which corresponds to 0.31 mW/GHz of power efficiency. Table II summarizes the performance of our PLL and compares it with other ULV PLLs using the

TABLE II
PERFORMANCE SUMMARY

Performance Parameter	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [8]	This work
Technology (CMOS)	180nm	130nm	90nm	130nm	65nm
Supply Voltage (V)	0.5	0.5	0.5	0.5	0.4
VCO type	LC-VCO	Ring-VCO	Ring-VCO	Ring-VCO	Ring-VCO
PLL Core Area (mm^2)	N/A	0.04	0.012	0.0736*	0.0081
Power (mW)	4.5	1.25	0.4	0.44*	0.109
Output freq. (GHz)	1.9	0.55	0.4	0.4-0.433	0.35
Ref. Spur (dBc)	-43.7	N/A	-40.28 @ 2.24GHz	-38.3	-55.3
RMS Jitter (ps)	N/A	8.01	9.62	5.5	30. 8
Phase Noise @ 1 MHz (dBc/Hz)	-120.4	-95	-87	-91.5	-90
Power effciency (mW/GHz)	2.368	2.272	1	1.016	0.31
Normalized FOM	N/A	18.8	1.56	1.72	1

*: Including pulse-swallow counter, excluding AFC circuit

normalized figure of merit (FOM). For this, the FOM defined in [20] as

$$\text{FOM} = \frac{\text{area}(\text{mm}^2)}{\left(\frac{\text{tech.}}{0.065}\right)^2} \cdot \left[\frac{\text{mW}}{\text{MHz}}\right]^{1.5} \cdot \left[\text{Jitter}_{\text{rms}}(\text{ps}) \cdot \sqrt{\text{mW}}\right]^2 \quad (1)$$

is used, where the area is normalized to 65-nm technology. For fair comparison, the areas of PLL cores that include PFD, CP, VCO, divider, and calibration circuits but not the loop filter are used for FOM comparison. As can be seen in the table, our PLL achieves the lowest reference spur, the smallest power efficiency, and the best FOM among recently reported ULV PLLs.

IV. CONCLUSION

We have demonstrated a 0.4-V, 90- to 350-MHz PLL in standard 65-nm CMOS technology. The CP in our PLL has an ALF architecture that operates well with ULV supply without current mismatch, resulting in a significant reduction in reference spur. It also has a VCO designed with the body-bias technique and includes an AFC circuit that provides low VCO gain with a wide tuning range. The PLL consumes only 109 μW for 350-MHz output.

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